**Task 6 (D2) unit 19 Explain how the width of the data bus and address bus affect processor performance and complexity.**

RAM

00

Address bus

CPU

01

10

As you can see the diagram each bus is equivalent to one bit also there is simply two buses shown on the diagram and this means only four addresses can be transferred.

11

**Introduction**: The performance and complexity of the processor is determined by the width of the data and address bus. So I will be explaining how address and data bus works with the Central processing unit and the Ram.

**Address bus**: The address bus transmits the address on where data wants to be passed towards or from the Ram. So if the address bus was one bit then there are only two likely memory slots where data can be collected from. For example, data can be composed from the address 0 or 1 also it cannot go outside that range.

Another example, if the address bus was 2 bit instead of 1 then the CPU can only access up to four memory slots such as 00,01,10,11. This shows that the width of the bus will be required to be lengthy so that there are extra locations for data to be collected from. The width of the address bus also controls how many bits on the memory address it can transfer.

So a wider address bus will improve a computer speed performance because the longer the address word pass along the address bus means it permits longer words and this makes extra memory to be addressed. On the other hand, if the width of the address bus is continuously increased then the motherboard will have a big problem supporting the amount of wires the bus might hold. This means there are extra memory slots on the Ram that memory cannot be addressed. Consequently, the only solution to the problem is to make sure the motherboard supports a particular amount of bits and the width of the address can be stored.

00001101

00001110

Data bus

RAM

CPU

00001111

As you can you the Width of the bus is 4 bit.

000101111

**Data bus**: The data bus is somewhat alike to the address bus however it works in a different method. The data bus has to fetch the data which is inside the RAM and it requires to be transported back to the CPU for processing. So the data bus must have the correct distance in order to transfer enough bits for the data to be transmitted via a memory slot in the RAM and transport it back to the CPU. An example, if the data bus was one bit, then it can transmit one bit of data at a certain time. This will have an impact on the performance of the processor because it will have to process one bit of data at a certain time and it will have to make eight cycles just to regain all the data from a memory slot, if there are extra lines this means fewer cycles will need to be processed.

An example, if we have a 4 bit which the speed is increased then it will be better than a 1 bit. However, it is not sufficient to process data that is bigger than 4 bits. Consequently, the width must be enlarged even further to transport extra bits of data. This means if processor is more powerful than it can transfer data between them more easily because of the speed of the clock is actually fast then the data bus it can create numerous cycles without hampering the performance of the CPU.

On one hand, it could have an impact on the processor since, the larger the bus the extra complexity of the interface circuits and the more 'wires' connecting the buses to the Ram and CPU. The performance of the computer system is controlled by how much gigahertz the computer is capable to process, which is the clock speed or even the bus width which controls how many buses are inserted to the motherboard.